WHAT IS CLAIMED IS:

1. A semiconductor switching device comprising: a multi-source FET (Tr5) that including a main electric field transistor FET (QA) and a reference FET (QB);

a reference current setting circuit (11) feeding a reference current (Iref) that including a constant component current (Irefc) and a transient component current (Ireft) to the reference FET (QB) such that a source potential (VSA) of the main FET (QA) obtained when a load current (ID) flowing the main FET (QA) is not within the range of an over-current containing a transient component is not lower than a source potential (VSB) of the reference FET (QB);

a voltage comparator (CMP1) detecting that the source potential (VSA) of the main FET is lower than the source potential (VSB) of the reference FET;

counters (4, 14) counting the number of times of vibration of the reference current (Iref) to a predetermined number of times on the basis of the detection of the voltage comparator (CMP1); and

a gate driving circuit (8) turning an OFF state of the main FET (QA) by counting of the counter.

2. The device as claimed in claim 1, wherein the voltage comparator (CMP1) detects that the source potential (VSA) of the main FET is not lower than the source potential (VSB) of the reference FET, whereby the gate driving circuit (8) turns ON the main FET (QA).

3. The device as claimed in claim 1, wherein vibration of the reference current (Iref) is generated by repetition of start of feeding the transient component current (Ireft).

4. The device as claimed in claim 1, wherein the starting time interval is equal to or less than a third predetermined time.

5. The device as claimed in claim 1, wherein vibration of the reference current (Iref) is generated by repetition of ON/OFF operation of the main FET (QA) and the reference FET (QB).

6. The device as claimed in claim 5, wherein counting of the counters (4, 14) is performed in a duration equal to or less than a second predetermined time.

7. The device as claimed in claim 5, further comprising a dummy voltage setting circuit (2).

wherein the repetition of the ON/OFF operation is that the voltage comparator (CMP1) detects that the source potential (VSA) of the main FET is the source potential (VSB) of the reference FET, whereby the gate driving circuit (8) turns OFF the main FET (QA) and the reference FET (QB);

the dummy voltage setting circuit (2) sets a first potential (potential at point A) lower than the source potential (VSA) of the main FET;

the voltage comparator (CMP1) detects that the source potential (VSB) of the reference FET lowering is lower than the first potential, whereby the gate driving circuit (8) turns ON the main FET (QA) and the reference FET (QB);

the dummy voltage setting circuit (2) sets a second potential (potential at point B) greater than the first potential (potential at point A); and

the voltage comparator (CMP1) detects that the source potential (VSB) of the reference FET rising is greater than the second potential, and is greater than the source potential (VSA) of the main FET, whereby the gate driving circuit (8) turns OFF the main FET (QA) and the reference FET (QB).

8. The device as claimed in claim 1,

wherein, in the case where the source potential (VSA) of the main FET is equal to the source potential (VSB) of the reference FET, a value is obtained as "n" when a load current (ID) flowing the main FET (QA) is divided by the reference current (Iref), and

wherein the reference current setting circuit (11) comprises:

a constant component circuit (14) feeding the constant component current (Irefc) that is greater than a value obtained by dividing by "n" a current value in a constant state when the load current (ID) is not within the range of an over-current; and

a transient component circuit (13) that flows the transient component current (Ireft) that is greater than a value obtained by dividing by "n", a current value of a transient component in a transient state when the load current (ID) is not within the range of an over-current.

9. The device as claimed in claim 8, wherein

the constant component circuit (14) feeding the constant component current (Irefc) is carried out when the load current (ID) flows.

10. The device as claimed in claim 1, wherein

the transient component circuit (13) feeding the transient component

current (Ireft) is that

the transient component circuit (13) is fed at the first predetermined time and at the predetermined current value;

the source potential of the reference FET is decreased within the range such that the source potential (VSA) of the reference FET does not exceed the source potential (VSA) of the main FET, and is set to be substantially zero within the second predetermined time after an elapse of the first predetermined time.

11. The device as claimed in claim 10, wherein

the transient component circuit (13) feeding the transient component current (Ireft) is started by the voltage comparator (CMP1) detecting that the source potential (VSA) of the main FET is lower than the source potential (VSB) of the reference FET, and is not started within the second predetermined time.

12. The device as claimed in claim 10, wherein

the predetermined number of times in the determined first time is less than the predetermined number of times in the second predetermined time.

13. An over-current shutdown method comprising:

a step A of feeding the reference current (Iref) that including the constant component current (Irefc) and the transient component current (Ireft) to the reference FET (QB) such that the source potential (VSA) of the main FET (QA) obtained when the load current (ID) flowing the main FET (QA) is not within the range of an over-current containing the transient component is not lower than the source potential (VSB) of the reference FET (QB);

a step B of detecting that the source potential (VSA) of the main FET is lower than the source potential (VSB) of the reference FET;

a step C of the reference current (Iref) vibrating by detecting in the step B,

a step D of counting the number of times of the vibration of the step C to the predetermined number of times; and

a step E of turning OFF the main FET (QA) by counting the step D.

14. The shutdown method as claimed in claim 13, further comprising:

a step F of detecting that the source (VSA) of the main FET is not lower than a source potential (VSB) of the reference FET: and

a step G of turning ON the main FET (QA) by detecting the step F.

15. The shutdown method as claimed in claim 13, wherein

the vibration of the step C is generated by a step H repeating the start of feeding the transient component current (Ireft).

16. The shutdown method as claimed in claim 15, wherein

the starting time interval is equal to or less than a third predetermined time.

17. The shutdown method as claimed in claim 13, wherein

the vibration of the step C is generated by a step I repeating the ON/OFF operation by the main FET (QA) and the reference FET (QB).

18. The shutdown method as claimed in claim 17, wherein

counting of the step D is performed in a duration equal to or less than the second predetermined time.

19. The shutdown method as claimed in claim 5, wherein

repeating the ON/OFF operation comprises:

a step J of turning OFF the main FET (QA) and the reference FET (QB) by detecting the step B;

a step K of detecting that the source potential (VSB) of the reference FET lowering is lower than the first potential (potential at point A) that is lower than a source potential (VSA) of the main FET;

a step L of turning ON the main FET (QA) and the reference FET (QB) by detecting the step K;

a step M of detecting that the source potential (VSB) of the reference FET rising is greater than the second potential (potential at point B) that is greater than the first potential (potential at point A); and

a step O of turning OFF the main FET (QA) and the reference FET (QB) by detecting the step M.

20. The shutdown method as claimed in claim 13,

wherein, in the case where the source potential (VSA) of the main FET is equal to the source potential (VSB) of the reference FET, a value is obtained as "n" when a load current (ID) flowing the main FET (QA) is divided by the reference current (Iref), and

wherein feeding a reference current (Iref) of the step A comprises:

a step P of feeding the constant component current (Irefc) that is greater than a value obtained by dividing by "n" a current value in a constant state when the load current (ID) is not within the range of an over-current;

and

a step Q of feeding the transient component current (Ireft) that is greater than a value obtained by dividing by "n", a current value of a transient component in a transient state when the load current (ID) is not within the range of an over-current.

21. The shutdown method as claimed in claim 21, wherein

feeding the constant component current (Irefc) of the step P is carried out when the load current (ID) flows.

22. The shutdown method as claimed in claim 1, wherein

feeding a transient component current (Ireft) of the step Q comprises:

a step R of feeding the transient component current (Ireft) at the first predetermined time and at the predetermined current value; and

a step S of decreasing the transient component current (Ireft) within the range such that a source potential (VSB) of the reference FET does not exceed the source potential (VSA) of the main FET within the second predetermined time after the first predetermined time has been elapsed, and setting the current to substantially zero.

23. The shutdown method as claimed in claim 10, wherein

feeding the transient component current (Ireft) of the step Q is that

the voltage comparator (CMP1) is started by the circuit detecting that the source potential (VSA) of the main FET is lower than the source potential (VSB) of the reference FET, and is not started within the second predetermined time.

24. The shutdown method as claimed in claim 22, wherein

the predetermined number of times in the determined first time is less than the predetermined number of times in the second predetermined time.